Remarks

Formal acceptance of the above amendments as a Submission in connection with the USPTO's RCE practice is respectfully requested.

The status of the claims are given hereinabove. Namely, previously allowed claims 1-9 were amended and claims 10-14 were newly presented. Examination and favorable action therefor of claims 1-14 is respectfully requested.

With regard to allowed claims 1-9, revisions were made thereto including editorial revisions for purposes of enhancing the clarity thereof as well as revisions particularly setting forth the byte length of specific write data. In a number of instances, also, the term "the" was substituted with a to specifically note the first occurrence of the set forth expression relating thereto. A further detailed discussion of the claims is included hereinbelow.

With regard to base claim 1, as now amended, the performing of data writing occurs following the receiving of data and, moreover, the writing of the first data to ones of the nonvolatile memory cells is performed without the presence of the first signal pulses throughout the period in which data writing of the first data is performed. As can be seen from one example operation such as it relates to Figs. 20-21 of the drawings, although not limited thereto, it is noted that the data writing of a selected memory cell is effected at a period (IV) in which the signal pulses from the first terminal (e.g., SC) do not occur. With regard to dependent claims 2 and 3, the revisions therein are of a minor formal nature. Regarding dependent claim 4, the set forth first data is now specifically defined as a data of 512 bytes in length. As it relates to base claim 1, terminals SC and I/O of the example embodiment in Fig. 20 relate to the set forth "first

terminal" and "second terminal," respectively, the internal controller CTRL relates to the set forth "controller" and the cell groups 11 relate to the "nonvolatile memory cells." With regard to the example timing chart shown in Fig. 21, it is noted that an address is received in the timing period (I) and in a subsequent period (III), the write data or "first data" is inputted at time of occurrence of the series of pulses inputted to terminal SC (or "pulses of a first signal"). With regard to the writing period (IV), it is further noted that pulses are not inputted to the terminal SC or "first terminal," consistent with claim 1.

Regarding the data writing verify operation such as set forth in claim 2, an example thereof is seen with regard to the time period T_{42} of the data write operation. Regarding dependent claim 3, the power generating circuit (e.g., 37, 38 in Fig. 20) used in connection with the generating of power during the performing of data writing is relating thereto. In this example, data writing/data rewriting is effected under the control of the internal controller CTRL. With regard to dependent claim 4, the "first data" is defined as being 512 bytes in length, and, moreover, an address information associated with the writing of data is capable of also storing data that has a length greater than 512 bytes, consistent with that originally disclosed (see the example discussion thereof on page 35, lines 6-14, of the present Specification).

Revisions of a somewhat similar nature were also effected with regard to claims 5-9. As to the invention set forth therein, Figs. 25-26 are an example illustration relating thereto, although not limited thereto. The invention according to claims 5-9 sets forth a scheme including plural nonvolatile memory arrays (e.g., 84 and 85 in Fig. 25), each containing a plurality of memory cells (e.g., 11). The operation of the nonvolatile memory shown in Fig. 26 is consistent with that

set forth in the claims. As in claim 1, data is written in the addressed memory cells of the first nonvolatile memory array at a time when "first signal pulses" are not inputted to the clock terminal SC or "first terminal," consistent with that shown in period (IV) in Fig. 26. Regarding the writing of the second data to the addressed memory cells of the second nonvolatile memory array (see claim 6), note writing period (IV') which shows that data is written in the memory cells of the second memory array without the inputting of the "first signal pulses" to the first terminal or clock terminal SC in Fig. 20. Regarding the verify operation in dependent claim 7 as well as the performing of an erase operation in memory cells of one nonvolatile memory array while performing a data writing in addressed memory cells of another nonvolatile memory array, as called for in claim 8, an example thereof can be seen with regard to period (IV, IV') in Fig. 26 of the drawings as it relates to the embodiment in Fig. 25, although not limited thereto. Regarding dependent claim 9, the invention therein further sets forth the byte length details associated with the "first data" and the "second data" as well as the write data byte length capability.

The invention set forth in new claims 10-14 also calls for a nonvolatile memory scheme consistent with that called for in claims 1+ and 5+, although presented in a somewhat modifying form therefrom. It is submitted, the previously presented claims, as currently amended, as well as the newly presented claims 10-14 are directed to a nonvolatile memory which is a clear and patentable improvement over that previously known. Also, in view of the earlier allowance of claims 1-9, and since the present amendments thereto are, basically, of an editorial formatting/further clarifying nature and, furthermore, since the additional claims call for featured aspects contained in claims 1-9,

although presented somewhat differently therefrom, examination as well as favorable action of all of the currently pending claims, i.e., claims 1-14, is respectfully requested.

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Respectfully submitted,
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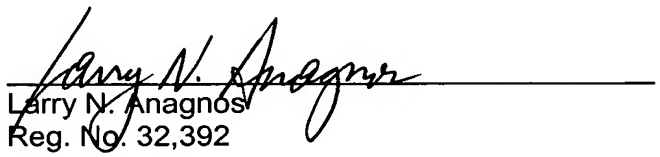

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